EDB7312 Development Kit

Hardware User's Manual

Embedded Processors Division

The information contained in this document is subject to change without notice.

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1 WARRANTY

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2 OVERVIEW

The EDB7312 (Cogent part number CSB238) was designed and developed by Cogent Computer Systems, Inc. for Cirrus Logic, Inc. as a highly Integrated EP73xx development platform. Based upon the Cirrus Logic, Inc. Maverick series of ARM processors, the EDB7312 provides a powerful, flexible platform for software design and development, hardware prototyping, embedded control systems, and more. The major features of the EDB7312 are:

- 74 MHz Cirrus Logic EP7312 Highly Integrated ARM Microprocessor
- Dual RS-232 Serial I/O
- Infrared Interface (115K baud)
- Integrated LCD Controller with interface to Optrex DMF-50944, 320x240 Color LCD Display
- 16 Mbyte SDRAM
- 16 Mbyte Intel E28F128 StrataFlash
- 8 Mbyte NAND FLASH
- Socket for 8-128Mbyte External Smart Media Card
- Bi-directional Parallel I/O Interface
- 16-Bit IDE Interface
- External Keypad Interface
- Intel 8042 PS/2 Keyboard/Mouse Controller
- Cirrus Logic CS8900A 10Mbit Ethernet Controller with 1 Kbyte EEPROM
- Burr-Brown AD7846 Touch Screen Controller
- Crystal CS53L32 24-Bit, CD Quality, Stereo Analog-Digital Converter
- Crystal CS43L42 24-Bit, CD Quality, Stereo Digital-Analog Converter with Integrated Headphone Amplifier
- Phillips Semiconductor PDIUSBD12 USB Peripheral Controller
- Built-in Macraigor “Wiggler” Interface for JTAG Based Debugging via the Parallel Port

3 ON-BOARD I/O DEVICES

3.1 EDB7312 ADDRESS MAP

The following table describes the Address Map of the EDB7312.

EP73xx Chip Select	Chip Select Width[6]	Default Wait States[6]	Address Start[1, 2, 3]	Address End	Description
CS0	16	5	0x00000000	0x00FFFFFF	16 Mbyte StrataFlash
CS1	8	2	0x10000000	0x10000000	On-Board NAND FLASH and SmartMedia Socket[5]
CS2	16	4	0x20000000	0x2000000F	CS8900A Ethernet Controller
CS2	16	4	0x20000300	0x2000030F	CS8900A PC-AT Compatibility Address
CS3	8	1	0x30000000	0x30000001	Parallel Interface Registers
CS3	8	1	0x30010000	0x30010000	Keyboard Extended Row Register
CS4	8	4	0x40000000	0x4000000F	PDIUSBD12 USB Controller
CS4	8	4	0x40010000	0x40010001	8042 PS/2 Keyboard/Mouse Controller
CS5	8/16[7]	1	0x50000000	0x50000006	IDE Interface
CS6[8]	32	0	0x60000000	0x600095FF	48 KByte SRAM
CS7[8]	32	0	0x70000000	0x7000007F	Boot ROM
N/A	N/A	0	0x80000000	0x80003FFF	EP73xx Registers
SDCS	32	N/A	0xC0000000	0xC0FFFFFF	16 Mbyte SDRAM

Table 1 – EDB7312 Address Map

Address Map Notes:

1. All addresses shown are physical addresses in normal (non-Boot ROM) mode. Refer to the EP73xx documentation for a description of the Chip Select mapping for Boot ROM Mode.
2. The EP73xx MMU may be setup to create different virtual address maps. Refer to the appropriate software documentation for any deviations from this map.
3. All addresses not listed here are reserved.
4. Many devices do not fully map their entire allotted address space. However, for future compatibility, do not access the devices outside of their address ranges listed here.
5. The On-Board NAND FLASH and the Smart Media Socket occupy one byte of address space. Selection of the desired device is done via EP73xx Control lines. Refer to Section 3.3 for more information.
6. Chip Select Width and Wait states are recommended values. Refer to the appropriate software documentation for detailed information regarding these values. Failure to adhere to

these values, however, may cause erratic behavior of the hardware.

7. CS5 must be placed in 8-bit mode when accessing the IDE Command and Status Registers. It must be placed in 16-Bit mode when accessing the IDE Data Register.
8. CS6 and CS7 are internal only and are described here for completeness purposes only.

3.2 16 MBYTE STRATAFLASH

The EDB7312 uses the Intel E28F128J3-150 StrataFlash device for boot memory. This device is enabled as 8M x 16. CS0 must be set to 16-bits width (this is the default on reset) and 5 wait states (the default is 8 wait states after reset). Refer to the "Intel StrataFlash Memory", Document Number #290667-006 for detailed programming information.

3.3 8 MBYTE NAND FLASH

The CS238 provides 8 Mbytes of built-in NAND FLASH using the Toshiba TC58V64AFT device. Note that this may be changed in future revisions to a different, but compatible vendor. This device is controlled using a number of EP73xx signals, including programmed I/O Port signals. The following table details the signal connections between the TC58V64 and the EP73xx.

TC58V64 Signal	EP73xx Signal	Notes
nCE	Port B Bit 6	Clearing Bit 6 sets nCE low to the TC58V64. Note that Port B Bit 7 must be high.
CLE	Port B Bit 4	Setting Bit 4 high, sets CLE high
ALE	Port B Bit 5	Setting Bit 4 high, sets ALE high
nRE	nOE & CS1	nRE goes low when nOE and CS1 are both true
nWE	nMWE & CS1	nWE goes low when nMWE and CS1 are both true

Table 2 – NAND FLASH Signal Assignments

Refer to the Toshiba TC58V64AFT Data Sheet for detailed programming information.

3.4 SMART MEDIA SOCKET

The EDB7312 allows the user to add additional NAND FLASH storage via the Smart Media Socket. This socket can accommodate any industry standard Smart Media (also known as SSFDC) card. Current cards provide from 8 Mbytes to 128 Mbytes of storage. The Smart Media Socket uses the same set of control signals as the on-board NAND FLASH with the exception that nCE to the Smart Media Socket goes low when Port B Bit 7 is low and Port B Bit 6 is high.

3.5 CS8900A ETHERNET CONTROLLER WITH 1 KBIT EEPROM

The CS8900A is used to provide the EDB7312 with a 10 Mbit Ethernet interface. The address map of the CS8900A is shown in the following table.

Address	Write Description	Read Description
0x20000000	Transmit Data, Port 0	Receive Data, Port 0
0x20000002	Transmit Data, Port 1 - 32-Bit Mode only, ***Do Not Use***	Receive Data, Port 1 - 32-Bit Mode only, ***Do Not Use***
0x20000004	Transmit Command	N/A
0x20000006	Transmit Length	N/A
0x20000008	N/A	Interrupt Status Queue
0x2000000A	Write Packet Page Pointer	Read Packet Page Pointer
0x2000000C	Write Packet Page Data Port 0	Read Packet Page Data, Port 0
0x2000000E	Write Packet Page Data Port 1 – 32-Bit Mode only, ***Do Not Use***	Read Packet Page Data Port 1 – 32-Bit Mode only, ***Do Not Use***

Table 3 – CS8900A Address Map

CS8900A Notes:

1. A 1 kbit EEPROM is attached to the CS8900A allowing for Non-Volatile storage for system parameters such as Ethernet MAC Address, routing tables, etc. Refer to the CS8900A Data Sheet for detailed information on accessing and programming the EEPROM.
2. Address lines SA8 and SA9 of the CS8900A are tied high, while SA4-SA7 and SA10-SA19 are all tied low. This causes the CS8900A to see addresses 0x00300 to 0x0030F only. This provides compatibility for software designed to work in a PC-AT ISA bus environment. Software may access the CS8900A at the EP73xx 0x20000300 base address or at 0x20000000.
3. CS8900A Interrupt output 0 is used to signal an interrupt to the EP73xx. This interrupt is routed to EINT3, which is shared with the Parallel Port. Software must setup CS8900A Interrupt 0 as level, high true.
4. Two LED's are provided to indicate the status of the Ethernet link. They are "Activity" and "Link". Refer to Section 6.3 for the location of these displays.

3.6 BI-DIRECTIONAL PARALLEL PORT

Implemented in logic is a simple bi-directional parallel port interface. This interface is fully software controlled and provides no additional support for various parallel port transfer modes. This interface consists of two 8-bit registers. The first, located at 0x30000000 is used to read/write the 8-data parallel port data bits. The second, at location 0x30000001 allows software to read/write the control/status signals as well as control the direction of the data register. The control/status register bit assignments are shown in the following table.

Bit	Write Description	Read Description
0	Set nPERROR Pin	Read state of nPERROR Pin
1	Set PE Pin	Read state of PE Pin
2	Set nACK Pin	Read state of nACK Pin
3	Set BUSY Pin	Read state of BUSY Pin
4	0 = Set Data Register Direction to Read 1 = Set Data Register Direction to Write	Read state of nSTROBE Pin
5	Set SLCT Pin	Read state of nAFD Pin
6	0 = Disable Parallel Port Interrupt 1 = Enable Parallel Port Interrupt	Read state of nSLCTIN Pin
7	Unused, must be 0	Read state of INIT Pin

Table 4 – Parallel Port Control/Status Register Bit Assignments

Parallel Port Notes:

1. For compatibility purposes, software may read/write the data and control registers using a single 32-bit read/write. As long as CS3 is setup correctly for 8-bits, the EP73xx will perform four 8-bit transfers. Newer software should do individual 8-bit reads/writes, as this will be a bit quicker since only two of the bytes are valid.
2. An option jumper is used to allow the Parallel Port to generate an interrupt to the EP73xx. One of four signals (nACK, nSTROBE, nSLCTIN or nINIT) may be selected, and when that selected signal is low, EINT3 (which is shared with the CS8900A Ethernet Controller) will be driven high. Refer to section 6.4 for detailed information regarding this jumper.

3.7 KEYBOARD EXTENDED ROW REGISTER

The Matrix Keyboard controller on the EP73xx provides 8 column bits and 8 row bits (Port A) thus allowing a maximum of 64 keys. In order to support larger arrays, an additional 8-bit register is provided to read another 8 rows, thus extending the maximum array size to 128 keys. Note that these rows cannot however, generate an interrupt as is possible with the Port A inputs. This register is located at 0x30010000.

3.8 USB CONTROLLER

The EDB7312 uses the PDIUSBD12 to provide a peripheral USB connection. The PDIUSBD12 supports all protocols as defined by the USB Standard, version 1.1. Software communicates with the PDISUBD12 via two 8-bit registers as shown in the following table.

Address	Write Description	Read Description
0x40000000	Write Data	Read Data
0x40000001	Write Command/Address	Read Status

Table 5 – PDIUSBD12 Address Map

PDIUSBD12 Notes:

1. The PDIUSBD12 Suspend status signal is routed to the EP73xx Port E Bit 1 input. When the PDIUSBD12 is in the suspend state, this bit will be 1.
2. The PDISUBD12 Interrupt output is routed to the EP73xx nEINT1 input. Note that this interrupt is shared with the 8042 PS/2 Keyboard/Mouse Controller.
3. A simple sense circuit allows the EP73xx to detect when a cable is connected to the EDB7312 and a powered-up Host. This sense line is routed into the PDIUSBD12 nEOT input and can be read via PDIUSBD12 Interrupt Register Byte 2, EOT Bit. When a cable is installed between the EDB7312 and a powered-up Host, this signal will be 1. If the Host is not powered-up, or if there is no cable installed, this signal will be 0. Refer to the PDIUSBD12 Users Manual for detailed programming information on accessing this bit.
4. DMA Mode is not supported and must not be enabled.

3.9 PS/2 KEYBOARD/MOUSE CONTROLLER

The EDB7312 uses the Intel 8042 (or equivalent) PS/2 Keyboard/Mouse Controller to provide an interface to a PS/2 compatible Keyboard and/or Mouse. Software communicates with the 8042 via two 8-bit registers as shown in the following table.

Address	Write Description	Read Description
0x40000000	Write Data	Read Data
0x40000001	Write Command/Address	Read Status

Table 6 – 8042 PS/2 Keyboard/Mouse Controller Address Map

8042 PS/2 Keyboard/Mouse Controller Notes:

1. The Output Buffer Full Flag is used to signal a Keyboard Port Interrupt. The Auxiliary Output Buffer Full Flag is used to signal a Mouse Port Interrupt. Both interrupts are tied to nEINT1 and are shared with the PDIUSBD12 USB Controller.

3.10 16-BIT IDE INTERFACE

The EDB7312 implements a 16-Bit IDE Interface using discrete logic. The following table describes the address map of an ATAPI compatible IDE device as seen via this interface.

Address	CS5 Mode	Write Description	Read Description
0x50000000	16-Bit	Write Device Data	Read Device Data
0x50000001	8-Bit	Features Register	Error Status Register
0x50000002	8-Bit	Sector Count Register	N/A
0x50000003	8-Bit	Sector Number Register	N/A
0x50000004	8-Bit	Cylinder Low Register	N/A
0x50000005	8-Bit	Cylinder High Register	N/A
0x50000006	8-Bit	Device Head Register	Error Status Register
0x50000007	8-Bit	Command Data Register	Status Register
0x5000000E	8-Bit	Device Control Register	Alternate Status Register
0x50010000	8-bit	Set IDE Mode to PIO Mode 3	N/A

Table 7 – 16-Bit IDE Interface Address Map

16-Bit IDE Interface Notes:

1. CS5 must be set to 16-bits when accessing the Data Register and set to 8-bits for all other accesses.
2. Any Addresses not shown are reserved and should not be accessed.
3. The IDE Interrupt output is connected to the EP7xx nEINT2 interrupt pin, which is shared with the AD7846 Touch Screen Controller.
4. The Expansion Clock Enable Bit in SYSCON 1 of the EP73xx Internal Registers must be set in order for this interface to work.
5. The IDE interface defaults to PIO Mode 0 timing (600ns per access) after reset. PIO Mode 3 timing (180ns per access) can be enabled by any write to address 0x50010000. Once selected PIO Mode 3 is enabled until the EDB7312 is reset.

3.11 16 MBYTE SDRAM

Two 4 Mbit x 16, 4-Bank SDRAMS are connected to the EP73xx SDRAM Controller. Refer to Section 5.6 for appropriate setup for these devices.

3.12 CS53L32, 24-BIT STEREO A/D

The CS53L32 allows the EDB7312 to convert analog audio input to digital format. It is beyond the scope of this document to provide detailed programming information on the CS53L32. However, the resources used to connect the CS53L32 to the EP73xx are described in Section 4.6.

3.13 CS43L42, 24-BIT STEREO D/A

The CS43L42 allows the EDB7312 to convert digital format audio data into 24-Bit analog audio. The CS43L42 provides line out audio as well as an integrated headphone amplifier. It is beyond the scope of this document to provide detailed programming information on the CS43L42. However, the resources used to connect the CS43L42 to the EP73xx are described in Section 4.6.

4 EP73XX ON-CHIP I/O DEVICES

4.1 OVERVIEW

The EP73xx has a wealth of on-chip peripheral devices as well as a number of user defined control lines. While it is beyond the scope of this document to provide detailed programming and interfacing information for the EP73xx on-chip peripherals, the following section describes the assignments for these devices and control lines as implemented on the EDB7312.

4.2 EP73XX CHIP SELECTS

As described in Section 3.1, the EP73xx Chip Selects are used to enable the various peripheral devices on the EDB7312. As a cross-reference they are described again in the following table.

Chip Select	Attached Device(s)	Notes
CS0	E28F128 STRATAFLASH	
CS1	On-Board NAND FLASH and Smart Media Socket	Selection is done via GPIO
CS2	CS8900A Ethernet Controller	Access to Serial EEPROM is via CS8900A
CS3	Parallel Port Interface and Keyboard Extended Row Register	Extended Row Register used in conjunction with Port A
CS4	PDIUSBD12 USB Controller and 8042 PS/2 Keyboard/Mouse Controller	
CS5	IDE Interface	

Table 8 – EP73xx Chip Select Assignments

4.3 EP73XX I/O PORT PIN ASSIGNMENTS

The EP73xx has four User Programmable I/O Ports. Their usage is described in the following table. Note that it is the responsibility of software to setup these Ports for the correct direction and default state. After Reset, all Ports are defined as inputs.

EP73xx Port	Bit	Direction	Use	Notes
A	0-7	IN	External Matrix Keyboard and Keypad Rows	PA0-5 are used for User Keys 1-6 on the CDK238 External Keypad
B	0	N/A	N/A	Unused on EDB7312
B	1	OUT	SIO 0 RTS Line	0 = Assert RTS to Host
B	2	IN	SIO 0 RI	0 = Host is Asserting RI
B	3	IN	SSI Header Pin 13	Unused on EDB7312
B	4	OUT	NAND CLE	1 = Assert CLE to NAND FLASH
B	5	OUT	NAND ALE	1 = Assert ALE to NAND FLASH
B	6	OUT	Unused	Must be cleared at all times
B	7	OUT	NAND FLASH/ Smart Media Select Bit	0 = Enable On-Board NAND FLASH 1 = Enable Smart Media Card
D	0	OUT	Diagnostic LED and Auto-Wakeup Disable	1 = Turn Diagnostic LED On and Disable Auto-Wakeup Circuit
D	1	OUT	LCD Contrast Voltage Enable	1 = Enable LCD Contrast Voltage Generator, Unused on EDB7312
D	2	OUT	LCD Enable	1 = Enable LCD Display
D	3	OUT	LCD Backlight Voltage Enable	1 = Enable LCD Backlight Voltage Generator
D	4	I/O	2-Wire SDA	Data Line for 2-Wire Serial Communications, Used with CS53L32 and CS43L43
D	5	OUT	2-Wire SCL	Clock Line for 2-Wire Serial Communications
E	0	OUT	CODEC Enable	1 = Enable CS53L32 and CS43L43, 0 = Hold CS53L32 and CS43L43 in reset
E	1	IN	USB Suspend Status	0 = PDIUSBD12 is in Suspend State
E	2	IN	Unused on EDB7312	

Table 9 – EP73xx Port Pin Assignments

4.4 EP73XX INTERRUPT PIN ASSIGNMENTS

The EP73xx has 4 external interrupt pins. The following table describes their usage on the EDB7312. Note that for shared interrupts, software is responsible for polling the devices to determine the actual source.

EP73xx Interrupt	Source	Notes
EINT1	PDIUSBD12 USB Controller and 8042 PS/2 Keyboard/Mouse Controller	
EINT2	AD7846 Touch Screen Controller and IDE Interface	
EINT3	CS8900A Ethernet Controller and Parallel Port	
EXTFIQ	SSI Header Pin 11	Unused on EDB7312

Table 10 – EP73xx Interrupt Pin Assignments

4.5 EP73XX LCD CONTROLLER

The EP73xx contains an On-Chip LCD Controller. While it is beyond the scope of this document to describe the complete operation of this controller, this subsection provides information regarding the connection of an Optrex DMF-50944 Color LCD to the EP73xx. Please note that the Optrex data sheet is provided on the CD that came with the EDB7312 development kit.

The following table describes the connection between the EP73xx LCD Control Pins and the DMF-50944. In order to support an 8-bit interface required by the DMF-50944, we latch the four EP73xx LCD Data bits on the falling edge of CL2 and present them with the unlatched bits to the DMF-50944. CL2 is divided by 2 and presented to the DMF-50944 as the pixel clock. Refer to Cirrus Logic Application Note AN179 for more information on this technique.

DMF-50944 Signal	EP73xx Source Signal	Notes
D0-D3	EP73xx DD0-DD3	LCD Character Data, D7 is the MSB, D0 is the LSB
D4-D7	Latched from EP73xx DD0-DD3 on falling edge of EP73xx CL2	
FLM	EP73xx FRM	First Line Marker
LP	EP73xx CL1	Line Pulse
CP	EP73xx CL2 divided by 2	Character Pulse

Table 11 – EP73xx to DMF-50944 LCD Signal Connections

4.6 EP73XX DIGITAL AUDIO INTERFACE

The EP73xx Digital Audio Interface (DAI) pins are used to connect the EP73xx to the CS53L32 and CS43L42 Stereo Audio devices. The following table describes the connection between the EP73xx and the two audio devices. Note that it is the responsibility of software to initialize the DAI interface for proper operation with the audio devices.

EP73xx Signal	Connection	Description
EXTCLK	11.2896 MHz Oscillator on EDB7312	
SDSYNC/ PCMSYNC	CS53L32 LRCLK CS43L42 LRCLK	Left/Right Synchronizing Clock
SDCK/ PCMCK	CS53L32 SCLK CS43L42 SCLK	Serial Bit Clock
SDTX/ PCMOUT	CS53L32 SDOUT	24-Bit Audio Input Data
SDRX/ PCMIN	CS43L42 SDIN	42-Bit Audio Output Data
Port D, Bit 4 2-Wire SDA	CS43L42 SDA CS53L32 SDA	2-Wire data for Configuration
Port D, Bit 5 2-Wire SCL	CS43L42 SCL CS53L32 SCL	2-Wire Clock

Table 12 – EP73xx Digital Audio Interface Pin Assignments

DAI Notes:

1. The 2-Wire protocol requires an address to be shifted to the slave devices. The CS43L42 is hardwired at 2-Wire address 0x10 and the CS53L32 is hardwired at 2-Wire address 0x11.

4.7 EP73XX SYNCHRONOUS SERIAL INTERFACE

The EP73xx Synchronous Serial Interface (SSI) is used to interface the EP73xx to the AD7846 Touch Screen controller. The following table describes the pin assignments for this interface.

EP73xx Signal	AD7846 Signal	Description
ADCCS	CS	Chip Select
ADCCLK	CLK	Serial Clock
ADCOUT	DIN	Command Data to AD7846
ADCIN	DOUT	Conversion Result Data from AD7846
SMPCLK	N/A	SSI Header Pin 1, Unused on EDB7312

Table 13 – EP73xx Synchronous Serial Interface Pin Assignments

4.8 EP73XX UARTS AND INFRARED I/O

The EP73xx has two UARTS for up to 115K-baud serial communications. UART1 supports full handshaking and is multiplexed with the Infrared Interface. UART2 supports no handshaking. Host communications in Boot ROM Mode uses UART1. The following table describes the EP73xx pins used for serial communications. Bit 15 (SIREN) in SYSCON1 of the internal EP73xx Registers is used to determine if UART1 is assigned to the Infrared Interface or to standard UART mode.

Serial I/O Signal	EP73xx Signal	Description
TXD1	TXD1	UART1 Transmit Data from EP73xx
RXD1	RXD1	UART1 Receive Data to EP73xx
DSR1	DSR1	UART1 Data Set Ready to EP73xx
DCD1	DCD1	UART1 Data Carrier Detect to EP73xx
CTS1	CTS1	UART1 Clear to Send to EP73xx
RTS1	Port B, Bit 1	UART1 Ready to Send from EP73xx
RI	Port B, Bit 2	UART1 Ring Indicator to EP73xx
IR_TX	IR_TX	Infrared Transmit Data from EP73xx
IR_RX	IR_RX	Infrared Receive Data to EP73xx
TXD2	TXD2	UART2 Transmit Data from EP73xx
RXD2	RXD2	UART2 Receive Data to EP73xx

Table 14 – UART and Infrared Pin Assignments

4.9 EP73XX RESET AND MODE CONTROL SIGNALS

The EP73xx supports a number of signals to provide various operating states. As a development system the EDB7312 allows the user to work with the EP73xx in these states. In order to do this, the signals for these states are brought out to a 16-pin header where they are designed to work with the CDK238 Membrane Keypad. The following table describes the connection between the EP73xx signals and the keypad.

EP73xx Signal	CDK238 Keypad Key	Description
nPOR	CPU POR	Pressing and releasing this key will assert a full reset to the EP73xx and the EDB7312.
nURST	CPU URST	Pressing and releasing this key will assert a User Reset to the EP73xx.
nBROM	CPU BROM	Holding this key down, while pressing and releasing CPU POR will place the EP73xx in Boot ROM Mode. At all other times, pressing and releasing this key will assert an FIQ to the EP73xx.
WAKEUP	CPU WAKEUP	Pressing this key will cause the EP73xx to move to the operating state if it was in the standby state.
nEXTPWR	CPU EXTPWR	Pressing this key will signal to the EP73xx that it is no longer operating on External Power.
nPWRFL	CPU PWRFL	Pressing this key will signal to the EP73xx that Power has Failed. This forces the EP73xx into the standby state
nBATOK	CPU BATOK	Pressing this key will signal to the EP73xx that Battery Power is no longer valid. It asserts an FIQ to the EP73xx.
nBATCHG	CPU BATCHG	Pressing this key will signal to the EP73xx that the Battery is below operating threshold.

Table 15 – EP73xx Reset and Mode Control Pin Assignments

5 EP73XX INITIALIZATION

5.1 OVERVIEW

Due to the various resources contained both on and off the EP73xx, it is necessary to initialize certain EP73xx registers before correct operation can begin. This section provides examples of this and can be used as a guideline. Note however, that failure to adhere to these guidelines may result in improper and even damaging behavior of the EDB7312 and/or EP73xx CPU.

5.2 PORTS A-E DIRECTION REGISTERS

These registers control the direction of the various Port pins. For Ports A, B and E, a one in a register bit will cause the corresponding pin to be an output, while a zero will cause the pin to be an input. For Port D, it is the opposite; a one will cause the corresponding bit to be an input, while a zero will cause the pin to be an output. Note that Port D defaults to all outputs, driven low after reset. A pin marked as I/O indicates that it may be re-assigned based upon the context of the current operation. This is most commonly used for data lines where reading and writing is required. The following table lists the recommended values for Data Direction Registers A, B, D and E. Refer to Section 4.3 for individual bit/pin assignments.

EP73xx Port	Default Value	Notes
A	0x00	All Inputs for Keyboard Scanning
B	0xF2	
D	PD4 In – 0x2F PD4 Out – 0x3F	PD4 is the 2-Wire Data Line, set to input as default, change to output only when needed
E	0x1	PE2 is unused, set as input

Table 16 – Port A-E Data Direction Register Default Values

5.3 SYSCON REGISTERS

There are three SYSCON registers that need to be set up for proper operation. Note that some of the modes and/or peripherals controlled by the SYCON registers need not be setup until they are needed. The values given here will only for those items that are required for proper operation. The following table lists the recommended default values for the SYSCON Registers.

Address	Default Value	Notes
SYSCON1@ 0x80000100	0x000411000	Enable UART1 (non-Infrared Mode), LCD Controller and External Clock Output
SYSCON2@ 0x80001100	0x00000102	Enable UART2, set SDRAM to 32-bits, set Keyboard Interrupt from Port A 0-5 only (USER1 to USER6 on CDK238 Keypad)
SYSCON3@ 0x80002200	0x0000020E	74 MHz Core Clock, 36 MHz Bus Clock, DAI Enable, 128 Frame/sec Mode

Table 17 – SYSCON1-3 Register Default Values

5.4 INTERRUPT MASK REGISTERS

It is recommended that all Interrupt Mask Registers be cleared (thus disabling all interrupts) until the appropriate interrupt handlers have been installed. Refer to the Software Users Manual for detailed information on the subject of Interrupts and Exceptions.

5.5 MEMORY CONFIGURATION REGISTERS

These two registers are used to setup the Chip Selects for size and wait states. The following table lists the recommended default values. Refer to Section 4.2 for individual Chip Select Assignments.

Address	Default Value	Notes
MEMCFG1@ 0x80000180	0x1F101710	CS0 – 16-bits, 4 Wait States CS1 – 8-Bits, 2 Wait State CS2 – 16-Bits, 4 Wait States CS3 – 8-Bits, 1 Wait State
MEMCFG2@ 0x800001C0	0x00001F13	CS4 – 8-Bits, 4 Wait States[2] CS5 – 8-Bits, 1 Wait State

Table 18 – MEMCFG1-2 Register Default Values

MEMCFG Notes:

1. The EDB7312 Boots the EP73xx in 16-Bit Mode. The values shown for MEMCFG1 and 2 reflect this. To use these values on another system requires adjusting the width field for each chip select based upon the actual Boot Width of that system.
2. CS5 is shown defaulted to 8-Bit mode, which is required for accessing the IDE Command and Control Registers. CS5 must be placed into 16-Bit mode when accessing the IDE Data Register. The value for SYSCON2 would then be 0x00001C13.
3. None of the default values set the Sequential Mode or Clock Enable Bits. Clock enable is handled in SYSCON1 and Sequential Mode is not appropriate for any of these devices.

5.6 SDRAM CONFIGURATION REGISTERS

Attached to the EP73xx SDRAM Controller are 4Mbit x 16, 4-Bank SDRAMs. In order for these devices to operate properly SDCONF and SDRFPR must be set correctly. The following table lists the recommended values.

Address	Default Value	Notes
SDCONF@ 0x80002300	0x00000522	CAS Latency = 2 64Mbit SDRAM Size 16-Bits per Device Always Enabled
SDRFPR@ 0x80002340	0x00000240	16usec Refresh period

Table 19 – SDRAM Configuration Registers Default Values

5.7 LCD CONTROLLER REGISTERS

The setup values given for the LCD Controller assume that an Optrex DMF-50944 320x240 Color Display (or equivalent) is attached. This display requires the use of external latching and clock dividing logic which is further described in Section 4.5. The following table describes the default values for this mode of operation.

Address	Default Value	Notes
LCDCON@ 0x80002C00	0xE60F7C1F	320x3x240 Display Size Pixel Clock Prescale = ÷ 2 AC Frequency = 13 Grayscale = 4-Bits/Pixel
PALLSW@ 0x80000580	0x76543210	Lookup Palette, Lower Word
PALMSW@ 0x80000540	0xFEDCBA98	Lookup Palette, Upper Word
FBADDR@ 0x80001000	N/A	Set to the start of the LCD Frame Buffer – Must be 115,200 bytes minimum
PCMCON@ 0x80000400	0x00000800	Set PWM1 to 96 kHz 50% Disable PWM0

Table 20 – LCD Configuration Registers Default Values

LCD Configuration Registers Notes:

1. The PWM function controlled by PCMCON is used to generate the LCD Contrast Voltage. To disable Contrast Voltage generation, write a 0 to this register. The default value provides a 96 kHz 50% duty cycle square wave. PWM0 is unused and should always be set to 0.
2. Each pixel in the display actually consists of three sub-pixels in the frame buffer, thus each byte in the Frame Buffer controls 2 sub-pixels, not 2 pixels.
3. Calculating an offset into the frame buffer from a Display Pixel Value is illustrated in the following code fragment:

```
//
   // Compute the display pixel number from the X and Y value
   //
  pixAdd = lX + (lY * 240); // 240 pixels per line

  // convert the display pixel number to a byte address.
  // Since we pack each pixel in 1.5 bytes we must multiply
  // the pixel address by 1.5.  Any remainder is saved and
  // flagged in pixRem

  pixRem = (pixAdd * 3) % 2;    // 1 if we had a remainder, 0 otherwise

  pucPtr = (unsigned char *)(HwLcdBaseAddress + ((pixAdd * 3)/2));

   //
   // Set the appropriate pixel based on the state of pixRem
   //
   if(pixRem)  // there was a remainder
   {
      // red is the higher nibble of the first byte

       *pucPtr = ((*pucPtr & 0x0F) | (color.r << 4));
        // Go to next byte, Green is lower, Blue is upper nibble
        pucPtr++;
       *pucPtr = ((*pucPtr & 0x00) | (color.g | (color.b << 4)));
   }
   else
   {
       // Red is lower nibble, Green is upper nibble in first byte
       *pucPtr = ((*pucPtr & 0x00) | (color.r | (color.g << 4)));
        pucPtr++;
       // Blue is lower nubble of the next byte
       *pucPtr = ((*pucPtr & 0xF0) | color.b);
  }
```

6 CONNECTORS, LEDS AND POTS

6.1 OVERVIEW

This section provides the locations, descriptions and pinouts of the various Connectors, Option Jumpers and Headers on the EDB7312.

6.2 CONNECTOR, JUMPER AND HEADER LOCATIONS – TOP SIDE

The following diagram shows the location of the connectors, option jumpers and headers on the top side of the EDB7312.

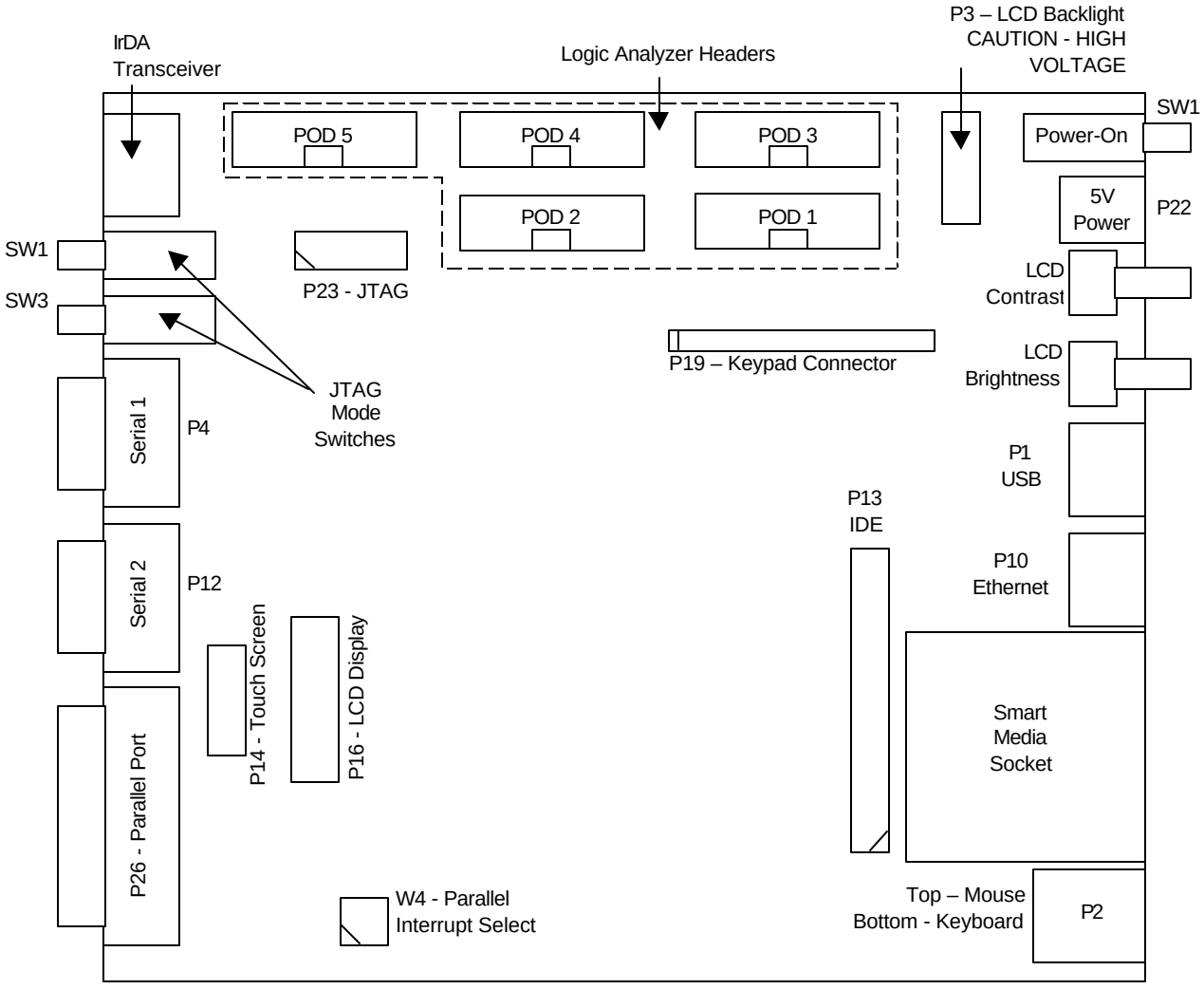

Figure 1 – EDB7312 Connector Locations, Top Side

6.3 CONNECTOR AND LED LOCATIONS – BOTTOM SIDE

The diagram below shows the orientation and location of the connectors and LED displays on the bottom of the EDB7312.

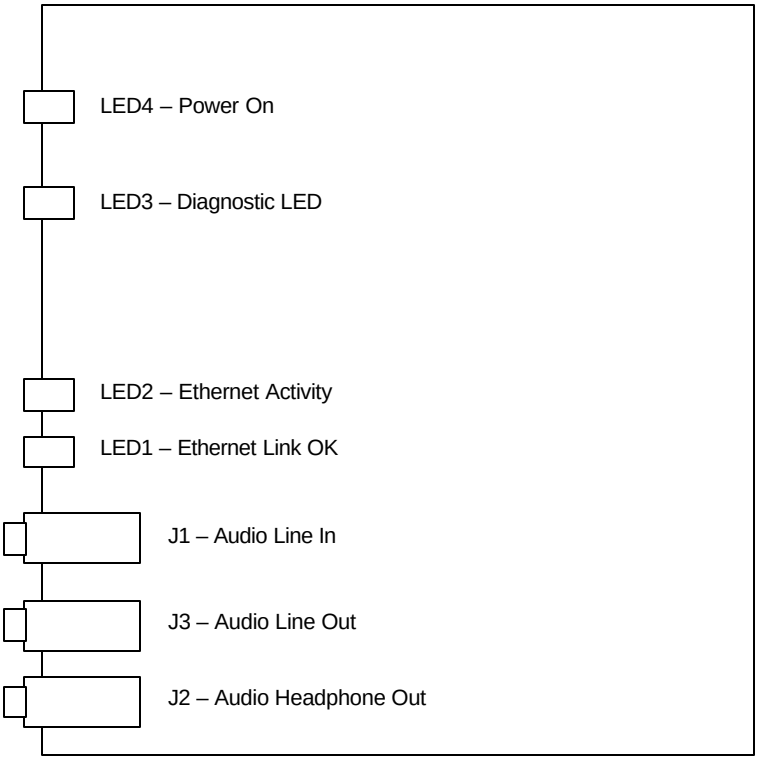

Figure 2 – EDB7312 Connector and LED Locations, Bottom Side

6.4 W4, PARALLEL PORT INTERRUPT SELECT

This 4-pin header allows the user to select the source for the parallel port interrupt on nEINT3. Note that in order for any interrupt to occur, software must set the Parallel Port Interrupt Enable Bit as shown in section 1.1. The following diagram shows the orientation of W4.

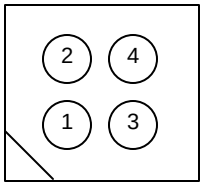

Figure 3 – Parallel Port Interrupt Select

The following table describes the Interrupt source associated with the four possible settings of W4.

Pins 1-3	Pins 2-4	Parallel Port Signal Used to Generate Interrupt
Jumper In	Jumper In	nSTB
Jumper In	Jumper Out	nAFD
Jumper Out	Jumper In	nSLCTIN
Jumper Out	Jumper Out	nINIT

Table 21 – Parallel Port Interrupt Source

6.5 P1, USB

P1 is a USB Type-B connector. The pinout for P1 is shown in the following table.

Pin	Signal	Description
1	USB_PWR	USB Power - Used only for Cable/Host sensing
2	D-	Data -
3	D+	Data +
4	GND	Ground

Table 22 – P1, USB Connector Pinout

6.6 P2, DUAL MINI-DIN CONNECTOR

P2 is a stacked Mini-DIN Connector used to interface to a PS/2 Keyboard and Mouse. The orientation of this connector is shown in the figure above. The following table provides the pinout for P2.

Pin	Signal	Description
1	DAT	Keyboard/Mouse Data
2	NC	No Connect
3	GND	Ground
4	VCC	+5V Power to Keyboard/Mouse
5	CLK	Keyboard/Mouse Clock
6	NC	No Connect

Table 23 – P6, Dual Mini-DIN Connector Pinout

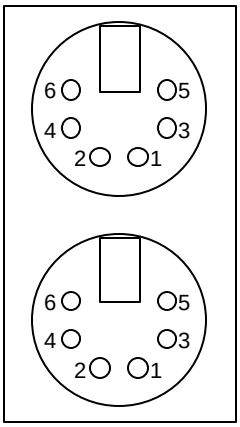

Figure 4 – P2, Dual Mini-DIN Connector

6.7 P4 AND P12, DB-9 MALE SERIAL CONNECTORS

P4 and P12 are used to connect to EP73xx UART 1 and UART 2. P4 supports full handshaking while P12 provides only TXD, RXD and Ground. The following table lists the pinouts for P4 and P12.

Pin	P4 Signal	P12 Signal
1	DCD	
2	RXD1	RXD2
3	TXD1	TXD2
4	DTR (Always = 1)	
5	Ground	Ground
6	DSR	
7	RTS	
8	CTS	
9	RI	

Table 24 – P4 and P12, DB-9 Pinouts

6.8 P10, RJ45 CONNECTOR

P10 is an 8-Pin RJ45 connector. It is designed to allow the EDB7312 to connect to a 10Mbit twisted-pair network. The pinout of this connector is shown in the following table.

Pin	Signal	Pin	Signal
1	TXD+	5	NC
2	TXD-	6	RXD-
3	RXD+	7	NC
4	NC	8	NC

Table 25 – P10, RJ45 Connector Pinout

6.9 P13, IDE CONNECTOR

P13 is a 40-pin Header designed to allow an IDE device to be attached to the EDB7312 via a 40-Pin ribbon cable. The pinout of this connector is shown in the table below.

Pin	Signal	Pin	Signal
1	nRST	2	Ground
3	Data Bit 7	4	Data Bit 8
5	Data Bit 6	6	Data Bit 9
7	Data Bit 5	8	Data Bit 10
9	Data Bit 4	10	Data Bit 11
11	Data Bit 3	12	Data Bit 12
13	Data Bit 2	14	Data Bit 13
15	Data Bit 1	16	Data Bit 14
17	Data Bit 0	18	Data Bit 15
19	Ground	20	NC
21	DMARQ (unused)	22	NC
23	nWR	24	Ground
25	nRD	26	Ground

Pin	Signal	Pin	Signal
27	IORDY	28	CSEL (unused)
29	nDMACK (unused)	30	Ground
31	NC	32	NC
33	Address Bit 1	34	NPDIAG (unused)
35	Address Bit 0	36	Address Bit 2
37	nCS0	38	nCS1
39	nDASP (unused)	40	Ground

Table 26 – P23, IDE Connector Pinout

6.10 P22, 2.1 MM POWER JACK

P22 is a standard 2.1mm DC-Jack used to provide power to the EDB7312. The center post is +5V while the outer ring is Ground.

6.11 P23, 14-PIN JTAG HEADER

P23 allows the user to connect a JTAG debugger to the EDB7312. The following table lists the pinout for P23.

14-Pin Header			
Pin	Signal	Pin	Signal
1	VDD (tied to +3V)	2	Ground
3	nTRST	4	Ground
5	TDI	6	Ground
7	TMS	8	Ground
9	TCLK	10	Ground
11	TDO	12	No Connect
13	VDD (tied to +3V)	14	Ground

Table 27 – P23, 14-Pin JTAG Header Pinout

6.12 P26, DB-25 PARALLEL I/O CONNECTOR

P26 is a right angle, female DB25 Connector. It is used to connect the EDB7312 to the Parallel Port of a Host Computer. The pinout of P26 is shown in the following table.

Pin	Signal	Pin	Signal
1	nSTROBE	14	nAFD
2	Data Bit 0	15	nPERR
3	Data Bit 1	16	nINIT
4	Data Bit 2	17	nSLCTIN
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	nACK	23	Ground
11	BUSY	24	Ground
12	PE	25	Ground
13	SLCT		

Table 28 – P26, DB-25 Parallel I/O Connector Pinout

6.13 J1, J2 AND J3, AUDIO JACKS

The CS53L32 24-Bit Stereo A/D receives its analog input via J1 (Line In). The CS43L42 outputs its analog data via J3 (Line Out) and J1 (Headphone Out). These connectors are standard 3.5mm Stereo Jacks.

6.14 LED DISPLAYS

LED1, LED2, LED3 and LED4 provide status information to the user. They are defined in the following table.

LED	Color	Status when On	Status when Off
1	Yellow	Ethernet Link is OK	Ethernet Link is Bad
2	Green	Ethernet is Transmitting and/or Receiving	Ethernet is not Active
3	Yellow	Auto-Wakeup Disabled	Auto-Wakeup Enabled
4	Green	Power is On	Power is Off

Table 29 – LED Display Assignments

6.15 RP1, LCD BRIGHTNESS AND RP2, LCD CONRTAST ADJUST

RP1 allows the user to adjust the brightness of the LCD backlight, while RP2 allows the user to adjust the LCD contrast for best viewing.

6.16 SW2, POWER SWITCH

SW2 is a momentary pushbutton switch. When depressed, SW2 energizes a latching relay, which in turn will route +5V from P22 to the EDB7312. Releasing SW2 does not remove power. You must remove the cord from the external Power Supply to remove power to the EDB7312. The EDB7312 uses a 3Amp Polyfuse to protect against short circuits. When a short occurs, the Polyfuse heats up and opens releasing the latching and removing power from the EDB7312. This allows the fuse to cool and eventually re-close. If SW2 were not a momentary switch, this closing of the fuse would cause power to be re-applied causing the sequence to begin again. The momentary switch insures that once the fuse has opened, power will not be automatically re-applied, thus improving the safety of the EDB7312.

6.17 SW1 AND SW3, JTAG MODE SELECT

SW1 and SW3 define the JTAG mode that the EP73xx will be operating in. The following table describes these modes. See Section 1 for more information on the built-in “Wiggler” interface.

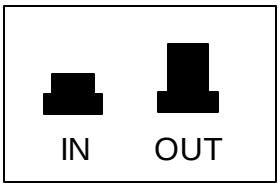

Figure 5 - Switch Positions

SW1	SW3	EP73xx Operating Mode
OUT	OUT	Normal Operation,Non-JTAG
IN	OUT	JTAG Debug via P23, 14-Pin Header
IN	IN	JTAG Debug with built-In “Wiggler” via P26, DB25 Connector
OUT	IN	Illegal, ***do not use***

Table 30 – JTAG Debug Switch Settings

7 MACRAIGOR "WIGGLER"

7.1 OVERVIEW

Built into the logic circuits of the EDB7312 is support for the Macraigor "Wiggler" JTAG interface. This low-speed connection allows the user to do basic JTAG based debugging without any additional hardware. The "Wiggler" interface is enabled via SW1 and SW3 and uses P23, the DB25 Parallel port connector. This method provides approximately 14Kbytes/sec download speed on the EP73xx. For faster JTAG interfaces (64Kbytes/sec and up), users are directed to the Macraigor web site (http://www.macraigor.com) for detailed information on the other JTAG options compatible with the EDB7312.

7.2 WIGGLER CONNECTION

The following steps describe the method for attaching and initializing the EDB7312 for "Wiggler" operation.

1. Remove power from the EDB7312.
2. Attach one end of the supplied 25-Pin Parallel Port Cable to the Host PC and the other end to P23 on the EDB7312.
3. Press SW1 and SW3 both in (see Section 6.17 for more detail).
4. Re-connect the Power Cable to P22 and press SW2, Power Switch.
5. After the board resets, you may begin to use your Host debugger to connect to the EDB7312 "Wiggler". Refer to the documentation for your debugger to determine the method for selecting the Macraigor "Wiggler" as the JTAG interface.

Note that when Macraigor "Wiggler" mode is enabled P23 is not available for Parallel Port use.

8 SOFTWARE MIGRATION

8.1 INTRODUCTION

The EDB7312 is designed to be highly compatible with the prior Cirrus Logic EP7209, EP7212 and prior version EP7312 Development Boards. However, since the EDB7312 is not 100% compatible with the EP72xx, this chapter details the differences and the implications for existing software. The previous chapters provide the necessary information on the actual details of the EDB7312 implementation. This chapter is primarily used to highlight those areas where change may be needed for proper operation.

8.2 BOOT-UP CODE

Boot-Up code is code that is run when the EP73xx first powers up. It is responsible for setting the chip selects and other EP7312 registers. The next sections detail specific areas of the boot code that may require modification.

8.2.1 CLOCK MODE AND RATE

The EDB7312 does not support external clock mode. It supports internal PLL mode only with the bus operated at 18 MHz or 36 MHz. Note however, that the EP73xx cannot achieve it's maximum internal operating rate unless the bus is at 36 MHz.

8.2.2 CS0 SIZE AND SPEED

The FLASH on the EDB7312 is an Intel 28F128 StrataFLASH. The speed of this device is 150 nsec, so the wait states should be set to 5. At a 36 MHz bus rate this gives an actual access time of 163 nsec. Also, unlike earlier Cirrus Logic Development Boards, the FLASH on the EDB7312 is 16-bits wide. The EP7312 boots up in 16-bit mode and this affects the rest of the chip selects. Boot code should be analyzed to insure that it sets the other chip selects accordingly.

8.2.3 CS1 NAND FLASH

The NAND FLASH (and the Smart Media Socket) on the EDB7312 is accessed as a single 8-bit port. Some earlier software from Cirrus Logic has setup the wait states for CS1 as 1, thus giving an access time of 54ns. The EDB7312 accesses the NAND FLASH via a buffer and this could cause problems if run at 1 wait state. We recommend setting the wait states for CS1 to a minimum of 2, thus giving an 81 nsec access time. This will have a negligible affect on performance.

8.3 LCD CONTROLLER

The LCD interface on the EDB7312 is optimized for the Optrex DMF-50944 320 x 240 color display. This device requires 8-bits of data. As described in earlier chapters, the LCD controller should be setup for gray scale, 4-bits per pixel (actually a sub-pixel: r, g or b). This gives 12-bits per actual displayed pixel. Most frame buffer drivers will not have a default mode for 12-bits per pixel and may require extensive modification.

8.4 TOUCH SCREEN INTERFACE

The EDB7312 uses the Burr-Brown ADS7846 touch screen controller. This device provides for simple scanning of the touch screen. Unlike the Cirrus Logic Development Boards, this controller eliminates the need for driving the touch screen with software, prior to testing for a touch. It also provides more accurate touch detection for interrupt generation. Any existing touch screen code will need to be modified, but in most cases this will mostly consist of simplifying and removing code.

8.5 IDE INTERFACE

The EDB7312 allows software to select PIO Mode 3 as well as PIO Mode 0 as was the default on the Cirrus Logic Development Boards.

8.6 PARALLEL INTERFACE

Unlike earlier boards, the EDB7312 implements the parallel port as two consecutive 8-bit registers. Setting CS3 to 8-bits (as recommended) allows code to access the parallel port as a single 16-bit port. The hardware will ignore accesses to any address other than the first two. Note that a 32-bit read or write to the parallel port will waste two cycles while the unused bytes are read or written.

8.7 MATRIX KEYBOARD

The EDB7312 provides the same interface to an external matrix keyboard as prior boards. However, the EDB7312 adds a PS/2 Keyboard/Mouse controller and this is the recommended keyboard interface for all new software. Future versions of the EDB7312 may not have the matrix keyboard interface at all.